A COMPLETELY ENCLOSED COPPER STRUCTURE TO AVOID COPPER DAMAGE FOR DAMASCENE PROCESSES

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to fabrication of copper damascene structures.

BACKGROUND OF THE INVENTION

As integrated circuit (IC) manufacturers move to copper (Cu) metallization for their most advanced products, protection of copper surfaces presents a big challenge for the back-end-of-line (BEOL) manufacturing processes. Copper damage, such as corrosion and oxidation, is often observed on wafers with open copper surfaces in the presence of moisture and/or acidic gasses.

Copper corrosion destroys the copper surface while copper oxidation results in poor adhesion both at Cu/barrier layer and Cu/stop layer systems. Copper oxide also enhances copper hillock during thermal processes.

U.S. Patent Nos. 5,380,546 and 5,451,551 both to Krishnan et al. describes a multilevel metallization process using polishing.

U.S. Patent No. 6,251,786 B1 to Zhou et al. describes a dual damascene interconnect with a silicon nitride (Si3N4) film 34 over the recessed dual damascene interconnect.

U.S. Patent No. 6,258,713 B1 to Yu et al. describes a dual damascene interconnect with a TiN layer over the planarized dual damascene interconnect.

U.S. Patent No. 6,274,499 B1 to Gupta et al. describes a dual damascene process with a dielectric cap 30.

U.S. Patent Nos. 6,114,246 to Weling, 6,103,625 to Marcyk et al. and 6,083,835 to Shue et al. are related patents describing barrier/CMP stop layers over damascene structures.

The article entitled "Finding the Ultimate Copper Barrier and Seed," Peters; Semiconductor International; July 2001; page 23, describes various barrier/liner materials such as WN, TaN, TaN + Co, TiN and TiN + PVD Cu.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide a copper damascene structure that protects the upper copper surface.

It is another object of one or more embodiments of the present invention to provide a method of forming a copper damascene structure that protects the upper copper surface.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure is provided having a patterned dielectric layer formed thereover. The patterned dielectric layer having an opening formed therein. A barrier layer is formed over the patterned dielectric layer, lining the opening. An initial planarized copper structure is formed within the barrier layer lined opening, and is planar with the barrier layer overlying the patterned dielectric layer. The initial planarized copper structure is recessed below the barrier layer overlying the patterned dielectric layer a distance to form a recessed copper structure. Any copper oxide formed upon the recessed copper structure is removed. A conductor film is formed over the recessed, copper oxide-free initial copper structure and the barrier layer. The excess of the conductor film is removed from over the barrier layer, and the

excess of the barrier layer overlying the patterned dielectric layer is removed, by a planarization process to form the planarized final copper structure. The planarized final copper structure comprising: the lower, recessed copper oxide-free initial copper structure; and an overlying planarized conductor film, wherein the overlying planarized conductor film isolates the lower, recessed copper oxide-free initial copper structure from the ambient atmosphere.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 4 schematically illustrates a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Initial Structure

As shown in Fig. 1, structure 10 has a dielectric layer 12 formed thereover. Dielectric layer 12 includes opening 14 exposing a portion of structure 10. Opening 14 may be, for example, a dual damascene opening as shown in the Figs. or a single damascene opening.

Structure 10 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Dielectric layer 12 is preferably comprised of a low-k material such as silicon oxide (SiO_2), FSG, a spin-on dielectric material, Black Diamond™ or nanoporous silica and is more preferably comprised of silicon oxide (oxide).

A barrier layer 16 is preferably formed over patterned oxide layer 12, lining dual damascene opening 14 to a thickness of preferably from about 50 to 1000Å and more preferably from about 50 to 300Å. Barrier layer 16 is preferably

comprised of tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), TaN + cobalt (Co), tantalum (Ta), titanium silicon nitride (TiSiN) or tantalum silicon nitride (TaSiN) and is more preferably TaN. TaN is more preferred because the addition of nitrogen (N) to tantalum (Ta) improves the stability of the barrier layer 16, possibly by segregation of nitrogen at the existing grain boundary.

An initial planarized copper structure 18 is formed within the barrier layer lined opening 14. If opening 14 is a dual damascene opening as shown in the Figs., then initial copper structure 18 is a planarized dual damascene structure, and if opening 14 is a single damascene opening, then initial copper structure 18 is a planarized single damascene structure. Initial planarized copper structure 18 is preferably formed using a copper chemical mechanical polish (CMP), stopping upon barrier layer 16.

Formation of Recessed copper Structure 18'

As shown in Fig. 2, initial planarized copper structure 18 is recessed 20 to form a recessed copper structure 18'. Copper structure 18 is preferably recessed 20 from about 180 to 500Å, more preferably from about 250 to 350Å and most preferably 300Å.

Initial planarized copper structure 18 is preferably recessed using a selective etch process employing an aqueous solution preferably comprising:

(1) NH_3/H_2O;

(2) $NH_3/H_2O_2/H_2O$;

(3) HNO_4/H_2O;

(4)HCl/H_2O; or

(5) H_2SO_4/H_2O;

and more preferably comprising $NH_3/H_2O_2/H_2O$.

When using the more preferred $NH_3/H_2O_2/H_2O$ aqueous solution to selectively etch initial planarized copper structure 18 to form recessed copper structure 18', the following reaction occurs:

$$Cu + 4\ NH_3 + 1/2\ O_2 + H_2O \rightarrow [Cu(NH_3)_4]^{++} + 2\ OH^-$$

where the copper complex $[Cu(NH_3)_4]^{++}$ product is formed on the top surface 19 of recessed copper structure 18'.

Removal of Copper Oxide from the Top Surface 19 of Recessed copper Structure 18'

The structure is then subjected to a reducing treatment to remove any copper oxide (CuO_x) from the surface 19 of recessed copper structure 18'. The reducing treatment includes a plasma containing Cu reducing agent such as preferably NH_3, H_2 or N_2, and is more preferably NH_3 or H_2. The reduction treatment may take place in situ in a physical vapor deposition (PVD) tool.

The following reduction reaction takes place, for example, to remove the copper oxide (CuO_x):

$$Cu^{++}O_x + 2\,H \rightarrow Cu + H_2O$$

This reduces formation of copper oxide and facilitates removal of copper oxide.

Conductor Film 22 Deposition

As illustrated in Fig. 3, a conductor layer 22 is deposited over recessed, copper oxide-free, initial copper structure 18' and barrier layer 16. The deposition of conductor layer 22 may be performed in situ in the same physical vapor deposition (PVD) tool as the copper-oxide-removal reduction treatment.

Conductor layer 22 is preferably comprised of tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), TaN + cobalt (Co), tantalum (Ta), TaSiN or TiSiN and is more preferably TaN.

Conductor layer 22 is preferably deposited by a PVD process or a CVD process and more preferably by a PVD process.

Planarization of Conductor Layer 22

As shown in Fig. 4, the structure is planarized to remove the excess of conductor layer 22 and barrier layer 16 from over dielectric layer 12 to form a planarized final copper structure 30 within opening 14 comprising: (1) a lower oxide-free initial copper structure 18' with (2) an overlying planarized conductor layer 22. The structure is preferably planarized using a CMP process.

Because the lower oxide-free initial copper structure 18' is completely enclosed/covered by overlying planarized conductor layer 22, copper corrosion and oxidation of planarized final copper structure 30 can be avoided due to its isolation from moisture (H_2O) and acidic gasses/vapors/liquids.

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. Cu oxidation is avoided;
2. Cu corrosion is avoided; and
3. Cu hillock is reduced.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.